Claims

I CLAIM:

1. A transmission line driving circuit comprising:

(a) a driver having an output;

(b) a transmission line having a proximal end and at least one distal end, the transmission line having an impedance;

(c) a series termination having a first terminal and a second terminal, the first terminal being connected to the driver output and the second terminal being connected to the transmission line proximal end; and

(d) a switch connected in parallel to the series termination, the switch operable when activated to change between a first, closed mode in which it operates as a substantially shorted circuit and a second, open mode in which it operates as a substantially open circuit.

2. The transmission line driving circuit of Claim 1 wherein the driver output is operably connected to a switch control terminal such that a rising-edged signal on the driver output will cause the switch to change to the second, open mode after a switching delay time no greater than twice the time needed for a signal to move from the proximal end of the transmission line to the at least one distal end of the transmission line.

3. The transmission line driving circuit of Claim 2 wherein the switching delay time is within plus or minus 20 percent of half of a rise time of the rising-edged signal on the transmission line driving circuit with an at least one load connected to the at least one distal end of the transmission line.

4. The transmission line driving circuit of Claim 2 wherein the transmission line driving circuit is configured such that the switching delay time

substantially satisfies the expression: $\frac{\Pi}{e}$ SquareRoot(((RC)^2 + T_{RISE} ^2)/2), where RC is a resistive-capacitive time constant of the transmission line driving circuit with the switch in the first closed mode, and at least one load is attached to the at least one distal end of the transmission line, and where T_{RISE} is the rise time of the rising-edged signal on the driver output.

5. The transmission line driving circuit of Claim 1 wherein the driver output is operably connected to a switch control terminal such that a falling-edged signal on the driver output will cause the circuit to change to the first, closed mode before the switch changes to the second, open mode.

6. The transmission line driving circuit of Claim 1 further comprising at least one receiver connected to the at least one distal end of the transmission line.

7. The transmission line driving circuit of Claim 1 wherein the series termination has an impedance that is substantially matched to the transmission line impedance.

8. The transmission line driving circuit of Claim 1 wherein the series termination is a resistor.

9. The transmission line driving circuit of Claim 1 wherein the switch is a FET switch.

10. The transmission line driving circuit of Claim 1 wherein the transmission line comprises a printed circuit board trace.

11. The transmission line driving circuit of Claim 1 wherein the switch is activated by a binary signal.

12. A method of controlling a transmission line reflection comprising the steps of:

(a) producing a short circuit across a first and second terminal of a source termination connected to a proximal end of a transmission line;

(b) employing a signal driver to apply a transitioning signal through the short circuit to the proximal end of the transmission line; and

(c) after applying the transitioning signal and before a signal reflection arrives from an at least one distal end of the transmission line, opening the short circuit.

13. The method of Claim 12 further comprising the step of pausing for a time delay before opening the short circuit.

14. The method of Claim 13 wherein the time delay is approximately one-half of an effective transition time of the transitioning signal in a circuit containing the driver, the transmission line, and an at least one load connected to the at least one distal end of the transmission line.

15. The method of Claim 13 wherein the time delay substantially satisfies the expression: $\frac{\Pi}{e}$ SquareRoot(((RC)^2 + T_{RISE}^2)/2), wherein RC is a resistive-capacitive time constant of the transmission line driving circuit, including at least one load attached to the distal end of the transmission line, RC being determined with short circuit existing across the series termination, and wherein T_{RISE} is a transition time of the transitioning signal as applied to the proximal end of the transmission line.

16. The method of Claim 13 wherein the step of pausing for a time delay is accomplished by opening the short circuit with a switch having a known switching delay time.

17. The method of Claim 12 wherein the step of producing a short circuit comprises closing a switch connected across the first and second terminals of the series termination.

18. The method of Claim 12 wherein the step of opening the short circuit comprises opening a switch connected across the first and second terminals of the series termination.

19. The method of Claim 18 wherein step of opening the short circuit is accomplished by applying the transitioning signal to a control terminal of the switch.

20. The method of Claim 18 wherein the step of opening the short circuit is accomplished by applying a driver input signal to a control terminal of the switch.

21. The method of Claim 12 wherein the step of producing the short circuit is accomplished by applying a falling-edged signal to the control terminal of the switch.

22. An adapting source termination circuit comprising:

(a) a control terminal;

(b) an input terminal;

(c) an output terminal;

(d) a transmission line having a proximal end, at least one distal end, and an impedance, the proximal end being connected to the output terminal; and

(e) wherein the adapting source termination circuit is operable to change a termination impedance, as measured between the input terminal and the output terminal, from a zero or near zero impedance to an impedance substantially matching the transmission line impedance after a transitioning signal is

applied to the input terminal and before a signal reflection arrives from the at least one distal end of the transmission line.

23. The adapting source termination circuit of Claim 22 further comprising:

(a) a resistor connected between the input terminal and the output terminal, the resistor having an impedance substantially matching the impedance of the transmission line; and

(b) a switch connected in parallel with the resistor, the switch having a switch control terminal, the switch control terminal being connected to the adapting source termination circuit control terminal.

24. The adapting source termination circuit of Claim 22 further comprising:

(a) a FET connected between the input terminal and the output terminal;

(b) a circuit adapted to apply a varying voltage on the gate of the FET in response to a signal on the control terminal to vary the drain-to-source resistance of the FET.

25. The adapting source termination circuit of Claim 22 wherein the control terminal is adapted to receive binary signals, the binary signals operable to cause the change in impedance.

26. The adapting source termination circuit of Claim 22 wherein the input terminal is connected to an output of a driver.

27. The adapting source termination circuit of Claim 26 wherein the driver has an output impedance of less than 2.5 ohms.

28. The adapting source termination circuit of Claim 22 wherein the control terminal is connected to an output of a driver.

29. The adapting source termination circuit of Claim 22 wherein the control terminal is connected to an input of a driver.

30. The adapting source termination circuit of Claim 22 wherein the change of termination impedance occurs after a delay time of approximately half of an effective transition time of the transmission line.

31. The adapting source termination circuit of Claim 22 wherein the change of termination impedance occurs after a delay time chosen to substantially satisfy the expression: $\frac{\Pi}{e}$ SquareRoot(((RC)^2 + T_{RISE}^2)/2) wherein RC is the resistive-capacitive time constant of the adapting source termination circuit with the zero or near zero impedance, including an at least one load attached to the at least one distal end of the transmission line, and wherein T_{RISE} is the transition time of the transitioning signal as applied to the input terminal.

32. A method of controlling a transmission line reflection comprising the steps of:

(a) driving a transmission line with a transitioning signal through a circuit with an impedance that is substantially zero;

(b) after substantially driving the transmission line and before a signal reflection arrives from a distal end of the transmission line, changing the impedance of the circuit from a substantially zero impedance to an impedance that substantially matches an impedance of the transmission line.

33. The method of Claim 32 further including the step of pausing for a time delay before changing the impedance.

34. The method of Claim 33 wherein the time delay is approximately one-half of an effective transition time of the transmission line.

35. The method of Claim 33 wherein the time delay substantially matches the expression: $\frac{\Pi}{e}$ SquareRoot(((RC)^2 + T_{RISE}^2)/2), wherein RC is a resistive-capacitive time constant of a circuit including the transmission line, a driver, and at least one load attached to the distal end of the transmission line, RC being calculated using the substantially zero impedance, and wherein T_{RISE} is a transition time of the transitioning signal as applied to the transmission line.

36. A reflection control driver comprising:

(a) a driver having a driver output;

(b) a controllable series termination having a first terminal, a second terminal, and a control terminal, the first terminal being connected to the driver output, the controllable series termination being configured to present a first short-circuit impedance between the first terminal and the second terminal in response to a first control signal being applied on the control terminal, the controllable series termination being configured to present a second impedance between the first terminal and the second terminal in response to a second control signal on the control terminal.

37. The reflection control driver of Claim 36 wherein the driver output is connected to the control terminal.

38. The reflection control driver of Claim 36 further comprising a driver input terminal on the driver, the driver input terminal being connected to the control terminal.

39. The reflection control driver of Claim 36 wherein the controllable series termination is configured to present the second impedance in response to the second input signal after a time delay.

40. The reflection control driver of Claim 39 wherein the time delay is at least a substantial portion of a transition time of a transitioning signal applied on the driver output.

41. The method of Claim 39 wherein the time delay is approximately one-half of an effective transition time of the transitioning signal in a circuit containing the reflection control driver, a transmission line, and at least one load connected to an at least one distal end of the transmission line.

42. The method of Claim 39 wherein the time delay substantially matches the expression: $\frac{\Pi}{e}$ SquareRoot(((RC)^2 + T_{RISE}^2)/2), wherein RC is the resistive-capacitive time constant of a circuit including the reflection control driver attached to a proximal end of a transmission line and at least one load attached to a distal end of the transmission line, RC being determined using the first short-circuit impedance, and wherein T_{RISE} is the transition time of the transitioning signal applied on the driver output.

43. The reflection control driver of Claim 36 wherein the controllable series termination further comprises:

(a) a resistor connected between the first and second terminals;

(b) a switch connected between the first and second terminals, the switch being operably connected to the control terminal.

44. The reflection control driver of Claim 43 wherein the switch is a FET.

45. The reflection control driver of Claim 36 further comprising a variable resistor connected between the first and second terminals and operatively connected to the control terminal.

46. A method of configuring a transmission line circuit comprising the steps of:

(a) finding an unloaded rise time of a driver;

(b) finding an expected total load capacitance C_{LOAD} on a transmission line;

(c) finding a desired rise time T_{LOAD} at a load;

(d) setting an impedance Z of the transmission line to substantially satisfy the expression $Z = sqrt(2)*T_{LOAD}/C_{LOAD}$ if the result of the expression is higher than a lowest practical Z value;

(e) setting the impedance Z of the transmission line to the lowest practical Z value if the result of expression $Z = sqrt(2)*T_{LOAD}/C_{LOAD}$ is lower than the lowest practical Z value;

(f) setting a series termination switching time T_S such that the driver transmits substantially all of a charge needed to charge C_{LOAD} onto the transmission line through a short circuit before time T_S.

47. The method of Claim 46, further including the step of setting a constant current driver to a current needed to drive substantially all of a charge needed to charge C_{LOAD} before time T_S.

48. A method of calibrating a circuit comprising the steps of:

(a) measuring a current out of a driver after a first reflection from a distal end of a transmission line has been dissipated;

(b) increasing a series termination switching time T_S if the current is non-zero.